A Low-Power 4.5–7.5-GHz Low Noise Amplifier–Phase Shifter Design

by

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A Diploma Thesis submitted in partial fulfillment of the requirements for the award of the Diploma in Electrical and Computer Engineering

Patras, Greece — October 2020
Nomenclature

ADC  Analog-to-Digital converter
ADS  (Keysight PathWave) Advanced Design System
CB   Common Base
CC   Common Collector
CE   Common Emitter
DAC  Digital-to-Analog converter
DSP  Digital Signal Processing/Processor
EM   Electromagnetic
ESD  Electrostatic Discharge
IL   Insertion Loss
LNA  Low Noise Amplifier
NF   Noise Figure
PA   Power Amplifier
PCB  Printed Circuit Board
PRF  Parallel Resonant Frequency
PS   Phase Shifter
RL   Return Loss
RTPS Reflection-Type Phase Shifter
Rx   Receiver
SMD  Surface-mounted Device
SPDT Single pole, double throw (switch)
SRF  Series Resonant Frequency
TL   Transmission Line
Tx   Transmitter
VGA  Variable Gain Amplifier
Abstract

This Thesis presents a low-power RF receiver (Rx) front end that incorporates a low-power Low Noise Amplifier (LNA) and a passive reflection-type Phase Shifter (PS) capable of continuous phase shift, operating in the 4.5–7.5-GHz band. The LNA topology comprises of a cascode stage that increases amplifier gain, while keeping DC power consumption and noise figure (NF) low, followed by an emitter follower which has impedance matching capabilities. The PS consists of two cascaded 3-dB quadrature hybrid couplers with variable LC loads, including, but not limited to varactor diodes. The proposed reflection-type PS load design leads to 360° phase shift range and a maximum insertion loss variation of ±3.3 dB. The LNA consumes 9.6 mW and the overall Rx front end has a gain of 16.25 ± 3.75 dB and noise figure lower than 1.78 dB. The printed circuit board has an area of 21.76 cm² = 9.42 cm × 2.31 cm.
Acknowledgements

First and foremost, I am profoundly grateful to my supervisor professor, Dr. Grigorios Kalivas, for his guidance and for entrusting me to carry this thesis project through as well as for his mentorship in various courses throughout my studies, which piqued my curiosity for Electronics. Special thanks also to Dr. Vasilis Kolios for his insightful remarks and helpful comments in the initial stages of this Thesis. I would also like to express my deep appreciation to Mr. Georgios Konidas for his invaluable advice and persistent help during this dissertation. Without his instructions and suggestions, this Thesis would not have been possible.

Last but not least, I am indebted to my friends and family for their love, emotional and financial support as well as my teachers for cultivating my unquenchable desire for knowledge.
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Chapter 1

Introduction

Wireless communication has undoubtedly enabled the majority of the technological achievements of the 21st century. From Wi-Fi and widespread videoconferencing in the era of COVID-19 to 5G technology and deep space communication, it is evident that telecommunications are at the forefront of the so-called "Fourth Industrial Revolution". Of particular interest to this Thesis is the introduction of Wi-Fi 6E in January 2020, when the Federal Communications Commission of the United States of America released 1,200 MHz of spectrum for commercial use in the 6 GHz band, thus demonstrating that the capabilities of said band are great. Furthermore, Phase Shifters such as the one designed in this thesis are an integral part of phased arrays, that is, arrays of antennae that are electrically steerable and are extensively used in radars, space probes and even in some Wi-Fi routers. A block diagram of an RF receiver front end is depicted in Figure 1.1.

In order to appreciate the significance of electronics in RF communication, one should first be familiarized with the basics of RF transceivers. Data,
Figure 1.1: An RF front end [7]

represented by a digital bitstream, are converted into analog signals that are amplified by a Power Amplifier so that they can be transmitted via the transmitter antenna. The produced electromagnetic waves are usually propagated by air or vacuum and their power density is diminished significantly with proportion to the square of the distance travelled. Thus, the receiver antenna detects a weak signal which is properly amplified by a Low Noise Amplifier and subsequently modified back into a digital bitstream. The block diagram of a typical RF transceiver is presented in Figure 1.2. As its name suggests, a Low Noise Amplifier ought to amplify the received signal in a manner that minimizes the noise it adds to it. The Friis formula for noise, shown in equation (1.1),

\[
F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \frac{F_4 - 1}{G_1G_2G_3} + \cdots + \frac{F_{n-1}}{G_1G_2\cdots G_{n-1}} \tag{1.1}
\]

reveals that the noise factor, \(F_1\), of the first stage of a multistage amplifier, shown in Figure 1.3, is the dominant term of the equation, therefore the first-stage amplifier contributes the most in the total noise factor, \(F_{\text{total}}\).
On the other hand, Phase Shifters are used to change the value of the phase angle of an input signal through another control signal that is often handled automatically by a computer. Phase Shifters require a great deal of trade-offs due to the vast number of constraints that have to be taken into account during design. Ideally, a Phase Shifter should provide low insertion loss and insertion loss variation vs. frequency, low group delay and sufficiently large phase control range.
1.1 Objectives of this Thesis

The goal of this Thesis is to design a 6 GHz low-power Low Noise Amplifier for ultra-wideband receivers and a Phase Shifter with a full 360° phase control range and an acceptable insertion loss and insertion loss variation vs. frequency. As with every new project, one has to specify the performance goals of the design from the beginning. The objectives that were determined to be appropriate for this application are summarized in Table 1.1.

<table>
<thead>
<tr>
<th>Measures</th>
<th>Values</th>
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<td>Noise Figure</td>
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<tr>
<td>LNA-PS Gain</td>
<td>&gt; 10 dB</td>
</tr>
<tr>
<td>Input/Output Return Loss</td>
<td>&gt; 10 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>≈ 3 GHz</td>
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<tr>
<td>Phase Control Range</td>
<td>= 360°</td>
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<tr>
<td>Insertion Loss variation</td>
<td>as small as possible</td>
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Table 1.1: Objectives of this Thesis

The EDA software that was used in every step of the design process was PathWave Advanced Design System (ADS) by Keysight.
Chapter 2

Theoretical Considerations

Before we delve into the various stages of the design process, the first order of business is to establish some basic theoretical concepts that are related to Low Noise Amplifiers and Phase Shifters.

2.1 Microwave Theory

![Two-port network representation](image)

Figure 2.1: Two-port network representation [8]

Circuits, represented by two-port networks such as the one depicted in Figure 2.1, cannot be accurately described by the lumped-element model in high
Figure 2.2: (a) A distributed circuit model for a transmission line (b) a section $\Delta x$ of the transmission line [8]

frequencies. The reason behind this is that the wavelength of the voltages and currents in different parts of the network is a multiple of its physical dimensions. Therefore, the values of these quantities are varied and can no longer be considered constant over time. Likewise, wires cannot be considered mere lumped interconnects between components in the circuit, so the concept of transmission lines is introduced.

Figure 2.2 shows a transmission line connecting a voltage source, $V_s$, and a source impedance, $Z_s$, with a load impedance, $Z_L$, which is depicted as two separate parallel conductors. The transmission line model of the wire may be divided into infinitesimal sections $\Delta x$ which can in turn be modelled as lumped two-port networks. Each section comprises of the following quantities:

- $R = \text{series resistance per unit length, for both conductors, in } \Omega/m$
- $L = \text{series inductance per unit length, for both conductors, in } \text{H/m}$
- \( G = \) shunt conductance per unit length, in S/m (due to dielectric loss and the bulk conductivity of the dielectric material)

- \( C = \) shunt capacitance per unit length, in F/m

The equations that relate the voltages and currents in the network are called Telegrapher’s equations. They are presented below:

\[
\frac{\partial v(x, t)}{\partial x} = -Ri(x, t) - L\frac{\partial i(x, t)}{\partial x} \tag{2.1}
\]

\[
\frac{\partial i(x, t)}{\partial x} = -Gv(x, t) - C\frac{\partial v(x, t)}{\partial x} \tag{2.2}
\]

In the case of a steady-state with sinusoidal inputs, equations (2.1) and (2.2) are transformed into:

\[
\frac{dV(x)}{dx} = -(R + j\omega L)I(x) \tag{2.3}
\]

\[
\frac{dI(x)}{dx} = -(G + j\omega C)V(x) \tag{2.4}
\]

A quantity of critical importance, called characteristic impedance, is defined in equation (2.5).

\[
Z_o = \frac{V_o^+}{I_o^+} = \frac{V_o^-}{I_o^-} \tag{2.5}
\]

\( V_o^+ \) and \( V_o^- \) symbolize the amplitude of travelling waves of voltage in the \(+x\) and \(-x\) direction, respectively. Similarly, \( I_o^+ \) and \( I_o^- \) symbolize the amplitude of travelling waves of current in the \(+x\) and \(-x\) direction, respectively.

It may also be proven that:

\[
Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.6}
\]

The characteristic impedance of a transmission line is a real number when the line is lossless \((R = G = 0)\) and equal to \( Z_o = \sqrt{\frac{L}{C}} \).
The propagation constant, $\gamma$, is another noteworthy quantity. It is defined by the following governing equation:

$$\frac{V(x = 0)}{V(x = x)} = \frac{I(x = 0)}{I(x = x)} = e^{\gamma x} \quad (2.7)$$

It is a complex number that can be written as such: $\gamma = \alpha + j\beta$. The attenuation constant $\alpha$ represents the attenuation of the amplitude of the travelling wave due to ohmic losses, while $\beta$ represents the change of the phase of the travelling wave and is equal to its wavenumber, $\frac{2\pi}{\lambda}$. All in all, we can write that:

$$V(x) = V_o^+ e^{-\gamma x} + V_o^- e^{\gamma x} \quad (2.8)$$

$$I(x) = I_o^+ e^{-\gamma x} + I_o^- e^{\gamma x} \quad (2.9)$$

![Figure 2.3: A transmission line terminated in a load impedance $Z_L$ [15]](image)

Let us now turn to the case of a lossless transmission line terminated in a load impedance, whose geometry is shown in Figure 2.3. An incident travelling wave arriving from $x = -l$ to the load has a ratio of voltage to current equal to $Z_o$. Yet, the ratio of voltage to current at the load must be equal to $Z_L$. Consequently, it is derived that a portion of the incident wave will be reflected.
in order for this impedance mismatch to be reconciled. The reflected wave will propagate in the \(-x\) direction. A new measure is then defined as the voltage reflection coefficient:

\[
\Gamma = \Gamma(x = 0) = \frac{V_o^\prime}{V_o^\prime} = \frac{Z_L - Z_o}{Z_L + Z_o}
\]

(2.10)

that ranges from \(-1\) to 1. A quantity related to \(\Gamma\) is the voltage standing wave ratio (VSWR):

\[
\text{VSWR} = \frac{|V_{\text{max}}|}{|V_{\text{min}}|} = 1 + \left|\frac{\Gamma}{1 - |\Gamma|}\right|
\]

(2.11)

It falls in the range \([1, \infty]\). We may also compute the input impedance at any point of the transmission line through the equation below:

\[
Z_{\text{in}} = Z_o \frac{Z_L + jZ_o \tan \beta l}{Z_o + jZ_L \tan \beta l}
\]

(2.12)

It follows that for a short circuit at the load \((Z_L = 0)\), \(\Gamma = -1\) and \(Z_{\text{in}} = jZ_o \tan \beta l\), while for an open circuit \((Z_L = \infty)\), \(\Gamma = 1\) and \(Z_{\text{in}} = -jZ_o \cot \beta l\). Furthermore, if the length of the line is a half-wave \((l = \frac{\lambda}{2})\), then \(Z_{\text{in}} = Z_L\) for any value of \(Z_o\), whereas if we have a quarter-wave line \((l = \frac{\lambda}{4})\), it holds that \(Z_{\text{in}} = \frac{Z_o^2}{Z_L}\). Quarter-wave transformers, as they are alternatively named, have several applications, including in bias networks. Lastly, if \(Z_L = Z_o\), then \(\Gamma = 0\) and \(Z_{\text{in}} = Z_o\) for any \(l\) and \(\lambda\). In this case the transmission line is called matched and there are no reflected waves back into it.

### 2.1.1 S-parameters

Open or short circuit terminations used in Z-, Y-, H-, T- and ABCD parameters are quite difficult to realize in two-port networks in high frequencies. As a result, a new set of parameters has been established: the scattering
parameters, more commonly referred to as S-parameters. For an arbitrary N-port network, such as the one shown in Figure 2.4, the S-parameters are defined in the following form:

$$
\begin{bmatrix}
V_1^- \\
V_2^- \\
\vdots \\
V_N^-
\end{bmatrix} =
\begin{bmatrix}
S_{11} & S_{12} & \cdots & S_{1N} \\
S_{21} & S_{22} & \cdots & S_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
S_{N1} & S_{N2} & \cdots & S_{NN}
\end{bmatrix}
\begin{bmatrix}
V_1^+ \\
V_2^+ \\
\vdots \\
V_N^+
\end{bmatrix}
$$

(2.13)

where:

$$S_{ij} = \frac{V_i^-}{V_j^+} \bigg|_{V_k^+ = 0 \text{ for } k \neq j}$$

(2.14)

In other words, for $i \neq j$, the element $S_{ij}$ represents the contribution of an incident wave $V_j^+$ at port $j$ to the reflected wave $V_i^-$ at port $i$, with every other port being matched ($V_k^+ = 0$). Moreover, for $i = j$, the element $S_{ii}$ is
equal to the reflection coefficient of port $i$, which is virtually the percentage of the incident wave $V_i^+$ that is reflected by port $i$. S-parameters are complex numbers that can be written as phasors: $|S_{ij}|e^{j\phi}$; the angle $\phi$ indicates a phase shift of the signal due to its transmission through the network or its reflection by a port of the network.

For a two-port amplifier stage, the S-matrix reduces to:

$$
\begin{bmatrix}
V_1^- \\
V_2^-
\end{bmatrix} =
\begin{bmatrix}
S_{11} & S_{12} \\
S_{21} & S_{22}
\end{bmatrix}
\begin{bmatrix}
V_1^+ \\
V_2^+
\end{bmatrix}
$$

(2.15)

If port 1 is the input port and port 2 is the output port, then $S_{ii}$ elements represent the input and output reflection coefficients, $S_{21}$ is the gain of the amplifier stage and $S_{12}$ is related to the isolation of the network, i.e. the attenuation of spurious signals from the output to the input.

### 2.1.2 The Smith Chart

The Smith chart, presented in Figure 2.5, depicts the complex plane of the reflection coefficient,

$$
\Gamma = \frac{Z - Z_o}{Z + Z_o}
$$

(2.16)

for every value of impedance $Z$ with non-negative real part. Let $z$ be the normalized impedance:

$$
z = \frac{Z}{Z_o} = \frac{R + jX}{Z_o} = r + jx
$$

(2.17)

Thus we can write:

$$
\Gamma = \frac{z - 1}{z + 1}
$$

(2.18)

It follows that, if $Z = Z_o$, then $z = 1 \Rightarrow \Gamma = 0$, thus the origin of the Smith chart (red dot in Figure 2.5) corresponds to $z = 1$. By extension,
Figure 2.5: The Smith Chart

the horizontal axis represents real impedances with zero imaginary part. We may also write:

\[ \Gamma = U + jV = \frac{(r - 1) + jx}{(r + 1) + jx} \]  \hspace{1cm} (2.19)

Two new equations are derived from equation (2.19):

\[ \left( U - \frac{r}{r + 1} \right)^2 + V^2 = \left( \frac{1}{r + 1} \right)^2 \]  \hspace{1cm} (2.20)

\[ (U - 1)^2 + \left( V - \frac{1}{x} \right)^2 = \left( \frac{1}{x} \right)^2 \]  \hspace{1cm} (2.21)
Equations (2.20) and (2.21) refer to families of constant resistance and constant reactance circles, respectively, that are presented in Figure 2.6a and 2.6b.

(a) Constant resistance circles  
(b) Constant reactance circles  

(c) Conversion of $z = 1 + j1$ to $y = \frac{1}{z} = 0.5 - j0.5$

Figure 2.6: Circles and admittances on the Smith chart [8]

Admittances can be plotted in the Smith chart, too. Every antipodal point of a normalized impedance matches its normalized admittance. An example is shown in Figure 2.6c. As a result, a Smith chart depicting impedances, also known as $Z$ Smith chart, can be rotated by 180° so that it represents admittances. The new Smith chart is called $Y$ Smith chart.

It is important to mention that circles centered at the origin are called con-
stant VSWR circles that are associated with points with a constant $\Gamma$ value. Clockwise movement along a constant VSWR circle yields the normalized input impedance of a loaded transmission line with length specified by the values on the outer circle.

### 2.2 Low Noise Amplifiers

Having discussed at length the basics of Microwave Theory, this section of the Thesis addresses some theoretical considerations about Low Noise Amplifiers. A typical microwave amplifier block diagram appears in Figure 2.7.

![Typical microwave amplifier block diagram](image)

**Figure 2.7: Typical microwave amplifier block diagram [8]**

The reflection coefficients mentioned in Figure 2.7 are associated with the impedances looking at the ports indicated by the respective arrows.

#### 2.2.1 Noise

In electronics, what we mean by noise is random fluctuations, errors or interferences in a signal that may disrupt the information that it carries or corrupt
Noise types | Cause
---|---
Thermal noise of resistors | The ambient thermal energy causes random agitations of electrons in the conductor
Thermal noise of MOSFETs | Due to an innate gate resistance
Flicker / $\frac{1}{f}$ noise in MOSFETs | Due to slow fluctuations of the properties of the semiconductor
Shot noise in BJTs | Due to the transport of carriers across the base-emitter junction

Table 2.1: Noise types in electronic devices and their causes

its quality. Noise is caused by the electronic systems that an information signal passes through, environmental conditions or by external devices. Table 2.1 outlines the most commonly found types of noise caused by electronic components themselves.

While noise is described by a random process and we cannot compute its instantaneous value at a specific point in time, the average power of the noise signal remains constant over time. This leads to the signal-to-noise ratio, more commonly called as SNR:

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}}$$  \hspace{1cm} (2.22)

where $P_{\text{signal}}$ is the signal power and $P_{\text{noise}}$ is the noise power. If a signal passes through a noisy system, then the SNR will deteriorate. Therefore, noise factor, $F$, and noise figure, $NF$, are defined as such:

$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \Rightarrow NF = 10 \log F$$  \hspace{1cm} (2.23)

If a system is noiseless, then its noise figure is equal to $1 = 0$ dB.
Returning to Figure 2.7, it has been demonstrated in [8] that the minimum \(NF\) value that we can achieve depends solely on the value of \(\Gamma_s\), i.e. the value of the impedance that must be presented at the amplifier input. If \(\Gamma_s = \Gamma_{\text{opt}}\), then \(NF = NF_{\text{min}}\).

### 2.2.2 Amplifier Gain

We can rewrite equations (2.8) and (2.9) in the following way:

\[
V(x) = V_o^+ (e^{-\gamma x} + \Gamma e^{\gamma x}) \tag{2.24}
\]

\[
I(x) = \frac{V_o^+}{Z_o} (e^{-\gamma x} - \Gamma e^{\gamma x}) \tag{2.25}
\]

We may then calculate the time-average power in the transmission line as follows:

\[
P_{\text{avg}} = \frac{1}{2} \text{Re}\{V(x)I(x)^*\} = \frac{1}{2} \frac{|V_o^+|^2}{Z_o} (1 - |\Gamma|^2) \tag{2.26}
\]

The above equation indicates that, if a transmission line is not matched (\(\Gamma \neq 0\)) and reflections take place, then only a percentage of the incident power will be delivered to the load.

Now, we turn our attention to Figure 2.8. \(a_1, b_1, a_2\) and \(b_2\) are incident and reflected voltage travelling waves normalized to \(\sqrt{Z_o}\). Through the definition of S-parameters and for \(Z_o = 50 \, \Omega\), it holds that:

\[
b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.27}
\]

\[
b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.28}
\]

Since \(\Gamma_{IN} = \frac{b_1}{a_1} \) and \(\Gamma_{OUT}\big|_{E_x=0} = \frac{b_2}{a_2}\), we can deduce by substitution that:

\[
\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.29}
\]
Figure 2.8: A two-port microwave amplifier network [8] and:

\[
\Gamma_{\text{OUT}} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{2.30}
\]

The significance of equations (2.29) and (2.30) is that if reverse isolation \(|S_{12}|\) is not substantial, then any changes to the input matching network will also affect the performance of the output matching network. As a result, the two-port network is named bilateral. On the other hand, if \(S_{12} = 0\), then the unilateral assumption can be made and equations 2.29 and 2.29 are reduced to:

\[
\Gamma_{\text{IN}} = S_{11} \tag{2.31}
\]

\[
\Gamma_{\text{OUT}} = S_{22} \tag{2.32}
\]

The power input to the network is equal to:

\[
P_{\text{IN}} = \frac{1}{2} |a_1|^2 - \frac{1}{2} |b_1|^2 \tag{2.33}
\]

and the power delivered to the load is equal to:

\[
P_{\text{L}} = \frac{1}{2} |b_2|^2 - \frac{1}{2} |a_2|^2 \tag{2.34}
\]
Simultaneous conjugate match is attained when there is maximum power transfer from the source to the input and from the network and to the load. For this to occur, the following conditions must be met: \( \Gamma_{IN} = \Gamma_s^* \) and \( \Gamma_{OUT} = \Gamma_L^* \). Solving these equations concurrently yields the following \( \Gamma_s \) and \( \Gamma_L \) values:

\[
\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (2.35)
\]

\[
\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (2.36)
\]

where:

\[
B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (2.37)
\]

\[
B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (2.38)
\]

\[
C_1 = S_{11} - \Delta S_{22}^* \quad (2.39)
\]

\[
C_2 = S_{22} - \Delta S_{11}^* \quad (2.40)
\]

\[
\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (2.41)
\]

### 2.2.3 Matching Techniques

![Network Diagram](image)

Figure 2.9: A network used for matching a transmission line to a load impedance [15]

The aim of this section is to present methods and network topologies to match an arbitrary impedance to a transmission line with a real characteristic impedance, usually \( Z_o = 50 \, \Omega \).
Lumped-element Matching Networks

![Diagram of Lumped-element matching networks](image)

Figure 2.10: Lumped-element matching networks: (a) Network for $z_L$ inside the $1 + jx$ circle (b) Network for $z_L$ outside the $1 + jx$ circle [15]

The exact lumped-element matching network topology depends on the position of the normalized load impedance relative to the $1 + jx$ circle in the Smith chart, as explained by Figure 2.10. Figure 2.11 exhibits that by adding a series reactive component, the trajectory that the load impedance follows is on a constant-resistance circle, while if a shunt reactive component is added, then the trajectory of the load impedance is on a constant-admittance circle. Therefore, the design flow of such matching networks is based on calculating the value of the right-most component, so that the normalized impedance/admittance coincides with the $1 + jx$ circle on the $Z/Y$ Smith chart. Afterwards, the value of the second component is computed in such a manner that the impedance moves to the origin of the Smith chart ($z = 1$).

It is worth noting that resistive components in matching networks are inefficient in low-power designs due to their ohmic losses, so they are rarely used in RF design.

The main advantage of using lumped components is that the design of such matching networks can be simplified by using the graphical method summa-
Figure 2.11: Motions on the Smith chart due to series and shunt inductances and capacitances [8]

rized above. However, their main drawback is their narrowband behavior; impedance matching over a large bandwidth cannot be realized.

**Broadband Matching Networks**

Broadband matching networks can be constructed through the procedure described here. When either the source or the load impedance is a complex number, it is convenient to use an RLC equivalent impedance to approximate the frequency response of the port impedance of interest. A lumped
bandpass filter, such as the one in Figure 2.12, may then be produced that matches the real parts of the source and load impedances. Its parameters must be carefully tuned so that the reactive part of the frequency-dependent impedance is incorporated in the filter as one of its sections. Afterwards, the lumped components can be transformed into distributed transmission lines according to the equations provided in Figure 2.13 and [18].
2.2.4 Stability

Stability is of great concern in amplifier design, because uncontrolled oscillations in the system might disturb its intended behavior or damage its components irreversibly.

The necessary and sufficient conditions for unconditional stability are:

\[ |\Gamma_s| < 1 \] (2.42)

\[ |\Gamma_L| < 1 \] (2.43)

\[ |\Gamma_{IN}| = \left| \frac{S_{22}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \] (2.44)

\[ |\Gamma_{OUT}| = \left| \frac{S_{22}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1 \] (2.45)

A more convenient way to reduce the number of equations for unconditional stability is to introduce Rollet’s stability factor, \( K \), and stability measure, \( B_1 \). The conditions for unconditional stability now become:

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|^2} > 1 \] (2.46)

\[ B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \] (2.47)

where \( \Delta \) is given by (2.41).

2.3 Phase Shifters

Phase Shifters have numerous applications in RF design. They have beam-forming capabilities, thus they are widely used in RADARs or phased-array...
antennae. They are also extensively used in cancellation loops in Power Amplifiers, where high linearity is required, as well as in some measurement circuits.

A list of the basic key parameters and constraints related to Phase Shifters that need to be considered during design is presented below:

- **Phase control range**: usually $360^\circ$
- **Insertion loss**: if the PS is active, then gain can be achieved
- **Insertion loss variation versus phase**: if it is considerable and VGAs are not used, then amplitude distortion may occur
- **Bandwidth**: performance over frequency must remain consistent
- **Group delay**: large group delay variation means that broadband signals might experience distortion by effects, such as intersymbol interference
- **Chip/PCB size**: especially in application such as phased arrays, it is crucial that the physical dimensions, therefore also costs, are not excessive

### 2.3.1 Phase Shifter Types

**Vector Modulators**

Vector modulators are active circuits that can be used as Phase Shifters by weighting different signal paths. Each path provides fixed phase offsets and its gain is set by the control voltage of a VGA. These paths are then combined
together into an output signal that has been phase shifted accordingly. For example, in Figure 2.14a, the input signal is decomposed into its in-phase and quadrature components and the output signal magnitude and phase is given by

$$|V_{\text{out}}| = \sqrt{|V_0^\circ|^2 + |V_{90^\circ}|^2}$$  \hspace{1cm} (2.48)

and

$$\angle V_{\text{out}} = \arctan \frac{V_{90^\circ}}{V_0^\circ}$$  \hspace{1cm} (2.49)

Also, Figure 2.14b shows a vector modulator that has a $360^\circ$ phase shift capability. However, despite their excellent gain and phase controllability, vector modulators are not suited for low power applications due to their additive DC power consumption.

**Distributed Phase Shifters**

Distributed Phase Shifters, such as the one in Figure 2.15, are used to emulate slow-wave circuits, i.e. structures with reduced group velocity. The increased group delay results in phase shifted waves travelling each unit section. Unfortunately, large variable capacitance control ratio requires that a
trade-off be made between maximum phase control range and minimum insertion loss. Additionally, in order for a 360° phase range to be accomplished, a very large number of unit sections is required.

Reflection-Type Phase Shifters

Large variation of the values of reactive loads prompts large variation of insertion loss. So, 3-dB quadrature couplers are employed to realize reflection-type Phase Shifters. The output signal from the isolated port of the coupler is phase shifted because of reflections taking place between the variable loads and the through and coupled ports. The reflection coefficient, $\Gamma_T$, denoted...
in Figure 2.16 is given by:

\[ \Gamma_T = \frac{Z_T - Z_o}{Z_T + Z_o} \]  

(2.50)

Thus, the phase shift \( \Delta \phi \) is given by:

\[ \Delta \phi = 2 \left[ \arctan \left( \frac{|\text{Im}\{Z_{T,max}\}|}{Z_o} \right) - \arctan \left( \frac{|\text{Im}\{Z_{T,min}\}|}{Z_o} \right) \right] \]  

(2.51)

according to [5]. The variation of impedance \( Z_T \) is often realized through varactor diodes. Also, reactive loads are preferred in order for insertion loss to be at a minimum.

**Loaded-Line Phase Shifters**

![Loaded-Line Phase Shifter](image)

Figure 2.17: Loaded-Line Phase Shifter [20]

The electrical length of the transmission line, which determines the phase shift of the network in Figure 2.17, is given by:

\[ \theta_L = \arccos (-BZ_o) \]  

(2.52)

Such Phase Shifters are innately narrowband, despite providing a constant phase shift versus frequency.
Switched-Type Phase Shifters

Although the control signals of the previous types of Phase Shifters are analog voltages, a computer is required to drive them through a DAC, which might entail additional power consumption and chip area. Therefore, a digital Phase Shifter architecture may be implemented that circumvents the need for a DAC. Each section’s phase shift is a multiple of a minimum phase shift that defines the phase resolution. Then, each segment can be toggled at will by a digital bitstream via an SPDT switch. A 4-bit digital Phase Shifter example is shown in Figure 2.18. Usually, the respective phase shift sections are constituted of High-pass/Low-pass configurations or transmission lines, which are displayed in Figure 2.19 and 2.20. The differential phase shift for the switched-line phase shifter is equal to $\Delta \phi = \beta (L_2 - L_1)$, where $\beta$ is the propagation constant of the transmission line, according to [20].
2.4 Quadrature 3-dB Hybrid Couplers

\[
[S] = -\frac{1}{\sqrt{2}} \begin{bmatrix}
0 & j & 1 & 0 \\
1 & 0 & 0 & j \\
0 & 1 & j & 0 \\
\end{bmatrix}
\]  \hspace{1cm} (2.53)

3-dB quadrature hybrid couplers are directional couplers whose coupling factor is equal to 3 dB, that is, the signal power flowing through each output is half the input signal power. Moreover, the phase difference between the outputs is $90^\circ$. The power flowing in the isolated port is zero, when all ports are
matched. Ideally, the S-matrix of such couplers is given by equation (2.53). The most simple geometry of such couplers is the branch-line coupler, shown in Figure 2.21. However, they are not fit for wideband applications, because they exhibit a narrowband response.

An improved version of a hybrid coupler is the Lange coupler, whose layout is depicted in Figure 2.22. The connections between the dotted points is realized by bond wires, air bridges or even via transitions [11]. Also, its bandwidth may exceed one octave.

![Figure 2.21: A branch-line coupler [15]](image1)

![Figure 2.22: The Lange coupler [15]](image2)
2.5 Printed Circuit Boards

2.5.1 Microstrip

Figure 2.23: Cross-section of a microstrip transmission line

Microstrip is one of the most popular and versatile constructs that are used for transmission line implementations. As shown in Figure 2.23, microstrip is composed of a very thin conductor sheet that is printed on a grounded dielectric substrate. If the dielectric laminate is electrically thin, i.e. $H \ll \lambda$, then the propagated waves can be assumed that they are quasi-TEM waves. As a result, the phase velocity and phase constant are given by:

$$v_p = \frac{c}{\sqrt{\varepsilon_{\text{eff}}}}$$  \hspace{1cm} (2.54)

$$\beta = \beta_0 \sqrt{\varepsilon_{\text{eff}}}$$  \hspace{1cm} (2.55)

where $c$ is the speed of light in vacuum and $\beta_0$ is the phase constant of a TEM wave in vacuum. The effective dielectric constant, $\varepsilon_{\text{eff}}$, of the microstrip is given by:

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12 \left( \frac{H}{W} \right)}}$$  \hspace{1cm} (2.56)
Thus, we can derive the characteristic impedance of the microstrip transmission line given its physical dimensions via the following equation:

\[
Z_o = \begin{cases} 
\frac{60}{\sqrt{\varepsilon_{\text{eff}}}} \ln \left( \frac{8H}{W} + \frac{W}{4H} \right) & \text{for } \frac{W}{H} \leq 1 \\
\frac{120\pi}{\sqrt{\varepsilon_{\text{eff}}}} \left[ \frac{1.393 + 0.667 \ln \left( \frac{W}{H} + 1.444 \right)}{2} \right] & \text{for } \frac{W}{H} \geq 1 
\end{cases}
\] (2.57)

The reverse process is possible, too. Given the characteristic impedance and the effective dielectric constant, the required physical dimensions can be produced by:

\[
\frac{W}{H} = \begin{cases} 
\frac{8\varepsilon_{\text{eff}}^4}{\varepsilon_{\text{eff}}^4 - 2} & \text{for } \frac{W}{H} < 2 \\
\frac{2}{\pi} \left\{ B - 1 - \ln (2B - 1) + \right. \\
\left. \frac{1}{2\varepsilon_{\text{eff}}} \left( \ln (B - 1) + 0.39 - \frac{0.61}{\varepsilon_{\text{eff}}} \right) \right\} & \text{for } \frac{W}{H} > 2 
\end{cases}
\] (2.58)

where

\[
A = \frac{Z_o}{60} \sqrt{\frac{\varepsilon_{\text{eff}} + 1}{2}} + \frac{\varepsilon_{\text{eff}} - 1}{\varepsilon_{\text{eff}} + 1} \left( 0.23 + \frac{0.11}{\varepsilon_{\text{eff}}} \right)
\] (2.59)

\[
B = \frac{377\pi}{2Z_o\sqrt{\varepsilon_{\text{eff}}}}
\] (2.60)

### 2.5.2 Varactor Diodes

Varactor diodes are essentially reverse-biased pn junctions whose internal capacitance can be varied by an external control voltage which in turn vary the width of its depletion region. According to [2], the equation that describes the junction capacitance versus the reverse voltage, \( V_R \), is:

\[
C_J (V_R) = C_J (V_X) \left( \frac{V_R + \varphi}{V_X + \varphi} \right)^\gamma
\] (2.61)

where \( V_X \) is an arbitrary voltage, typically 0 V, \( \varphi \) is the built-in voltage of the pn diode and \( \gamma \) is a slope exponent which is equal to 0.5 for abrupt junction
and larger than 0.5 for hyperabrupt ones. The difference in capacitance change between abrupt and hyperabrupt diodes is shown in the diagram of Figure 2.24.

![Figure 2.24: C_J vs. V_R for an abrupt and C_J vs. V_R + \varphi for a hyperabrupt varactor diode [2]](image)

A varactor diode can also be described by an equivalent series circuit that is depicted in Figure 2.25.

![Figure 2.25: Series equivalent circuit for varactor diodes [2]](image)
Chapter 3

Narrowband Low Noise Amplifier Design

3.1 Transistor Selection

The first order of business is to select a reliable RF transistor that will be appropriate for this application and will produce satisfactory results in the operating frequency band of 4.5–7.5 GHz. After a thorough search and analysis of datasheets of prospective transistors, the list was narrowed down to two npn bipolar transistors: the NXP BFU910F and the Infineon BFP840FESD. Afterwards, their I-V characteristic curves were plotted using the ADS models provided by each company. These can be seen in Figures 3.1a through 3.1d.

Having calculated the $I_C-V_{BE}$ pairs for a given $V_{CE}$, we may now proceed to an S-parameter simulation for a basic Common Emitter configuration at 6
Figure 3.1: Infineon BFP840FESD and NXP BFU910F I-V characteristic curves

GHz, in order to obtain important quantities, including:

- $\text{NF}_{\text{min}}$: the minimum noise figure attained by presenting the optimal impedance, $Z_{\text{opt}}$ at the input
- $P_{\text{gain,assoc}}$: the gain associated with $\text{NF}_{\text{min}}$ when the input impedance is $Z_{\text{opt}}$ and the output is conjugate matched
- $\text{MAG}$: the maximum available gain, $\frac{|S_{21}|}{|S_{12}|} \left(K - \sqrt{K^2 - 1}\right)$, or the maximum stable gain, $\frac{|S_{21}|}{|S_{12}|}$, for $K = 1$, when both ports are conjugate matched
An example of the circuit topologies that were employed for the three Q-point cases for each of the two transistors is presented in Figure 3.2.

Figure 3.2: CE topology

The results of the S-parameter simulation are in Figures 3.3 and 3.4.
Figure 3.3: Infineon BFP840FESD unmatched CE topology simulation results for different Q-points
Figure 3.4: NXP BFU910F unmatched CE topology simulation results for different Q-points
Although, the NXP BFU910F provides better NF performance than its counterpart, its typical $V_{CE}$ value is 2.0V, whereas the latter transistor’s $V_{CE}$ value is 1.8V and can be safely lowered to 1.2V without the transistor risking to slip into saturation mode. Consequently, it was decided that the most suitable RF transistor for a low-power LNA is the Infineon’s BFP840FESD.

### 3.2 Common Emitter Topology with Emitter Degeneration

This section addresses the CE topology with narrowband-matched input and output ports for $f = 6$ GHz. This means that suitable impedances must be presented to the input and output of the transistor such that we achieve a desirable performance. At this stage, the matching networks shall be narrowband and will be designed using the method set out in subsection 2.2.3. Furthermore, an emitter degeneration inductor was added. According to [19] and [3], emitter degeneration feedback through an inductor instead of a resistor avoids additional ohmic losses. It also diminishes a trade-off between optimal noise figure and maximum gain, because it shifts $Z_{opt}$ closer to $50\Omega$. Slight improvement in stability occurs, too. This effect is depicted in Figure 3.5.

After fine-tuning the value, $L_E$, of the emitter degeneration inductor, it was calculated that its optimal value is 0.39 nH. We shall now examine three bias points for the foregoing configuration, that are shown in Table 3.1.

An example schematic of the new topology is shown in Figure 3.7. Also, the simulation results are presented in Figure 3.8, while the Smith charts that
Figure 3.5: Effect of emitter inductor on optimal noise figure admittance and constant-NF circles [3]

<table>
<thead>
<tr>
<th>$V_{BE}$ values</th>
<th>$I_C$ values</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8425 V</td>
<td>7.81 mA</td>
</tr>
<tr>
<td>0.82 V</td>
<td>3.63 mA</td>
</tr>
<tr>
<td>0.81 V</td>
<td>2.54 mA</td>
</tr>
</tbody>
</table>

Table 3.1: Three bias points for the CE topology with emitter degeneration for $V_{CE} = 1.8$ V

show the impedance transformation of the input and output ports are shown in 3.6.

The proximity of the input impedance to 50 Ω stems from the introduction of the emitter degeneration inductor, as discussed above. It is also observed that, after the incorporation of the inductor to the input/output impedance, the normalized admittance lies on the 1 + jb circle of the Y Smith chart (in red). Subsequently, the capacitor cancels the imaginary part of the impedance, so the input and output ports are matched to 50 Ω.

Several conclusions can be drawn from the results in Figure 3.8. For instance, noise figure increases steadily as the collector current, $I_C$, decreases. This is
(a) Input matching network:
\[ Z_{\text{in}}^* = 43.7065 + j21.9227 \, \Omega \]

(b) Output matching network:
\[ Z_{\text{out}}^* = 26.2537 + j50.7988 \, \Omega \]

Figure 3.6: Smith charts for the matching networks of Figure 3.7

Figure 3.7: Matched CE topology with emitter degeneration at \( V_{BE} = 0.82 \text{V} \)
corroborated by Figure 3.9, which reports that for a typical transistor with emitter length of 20 \( \mu \text{m} \), \( NF_{\text{min}} \) is optimal at an intermediate value of \( I_C \).
(a) Matching for minimum NF for $V_{BE} = 0.8425\ \text{V}, V_{CE} = 1.8\ \text{V}$

(b) Matching for maximum gain for $V_{BE} = 0.8425\ \text{V}, V_{CE} = 1.8\ \text{V}$

(c) Matching for minimum NF for $V_{BE} = 0.82\ \text{V}, V_{CE} = 1.8\ \text{V}$

(d) Matching for maximum gain for $V_{BE} = 0.82\ \text{V}, V_{CE} = 1.8\ \text{V}$

(e) Matching for minimum NF for $V_{BE} = 0.81\ \text{V}, V_{CE} = 1.8\ \text{V}$

(f) Matching for maximum gain for $V_{BE} = 0.81\ \text{V}, V_{CE} = 1.8\ \text{V}$

Figure 3.8: Matched CE configurations results with emitter degeneration for different Q-points
Also, amplifier gain falls markedly from 7.81 to 3.63 mA, but apparently levels off at $I_C = 2.54$ mA. Reverse isolation, represented by $S_{12}$, continues to be considerable, too, so the unilateral assumption, explained in subsection 2.2.2, cannot be made and broadband matching techniques cannot be applied. Therefore, alternative topologies will be explored to alleviate this obstacle. Lastly, stability degrades slightly while $I_C$ drops.

### 3.3 Cascode Topology

Due to the inferior reverse isolation and intrinsic conditional stability of the discrete transistor, the CE emitter configuration is an unacceptable solution for a broadband LNA design. So, the cascode (CE-CB) topology shall be explored. Aside from the superior reverse isolation, this topology lessens
the effect of the feedback caused by the Miller capacitance, thus offering wider operating bandwidth compared to a simple CE amplifier, as per [13]. On top of that, the power gain is increased further, since the amplifier now comprises of two stages that amplify both the current and the voltage of the input signal.

The schematic of the cascode LNA circuit is depicted in Figure 3.10. The operating point for this circuit is: $V_{BE}=0.82$ V, $I_C=3.61$ mA. $V_{CE}$ has been lowered from 1.8 V to 1.2 V, too; the transistors are still in the forward-active region of operation.

The reverse isolation, $|S_{12}|$, has nearly doubled in magnitude. However, the simulation results in Figure 3.11 show that the circuit is highly unstable and the reflection coefficients of the input and output ports exceed 1 (0 dB) at particular frequencies. For this reason, no other Q-points were explored. S-parameter matrices with elements $|S_{ii}| > 0$ dB translate to impedances...
Figure 3.11: Unmatched Cascode LNA topology simulation results

with negative real part. Their physical significance is that the amplitude of signals which will be potentially reflected at either port is liable to grow exponentially, thus unwanted oscillations will occur. This is explained in [21] and also verified in Figure 3.11 where the base impedance of the CB-stage transistor has negative real part. That result was produced by the "SP_Probe" component provided by ADS. Consequently, an alteration of the circuit that remedies the instability must be made.

The first attempt at a stable cascode configuration is presented in Figure 3.12. The output shunt resistor placement is a common practice in stabilizing two-port networks, that is outlined in [8]. It provides a satisfactory trade-off between gain and stability, i.e. stability improves substantially without the amplifier gain deteriorating. Also, narrowband lumped matching networks have been included and the emitter degeneration inductor, $L_E$, has been
Figure 3.12: Matched Cascode LNA topology with output shunt resistor ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)

Figure 3.13: Matched Cascode LNA topology with output shunt resistor simulation results ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)
adjusted accordingly to incorporate the changes induced by the resistor and the new topology. The updated simulation results are shown in Figure 3.13.

The placement of a resistor in series with the base of transistor $Q_2$ was also attempted, but, in order to attain adequate stability near 6 GHz, a large value of resistance was required. As a result, this method was abandoned.

### 3.4 Cascode – Emitter Follower Topology

Resistors are by nature lossy and noisy elements. So, we shall investigate a cascode topology where the output shunt resistor is replaced by an emitter follower, that is, a transistor in common collector configuration. [19] illustrates that common-collector amplifiers operate as voltage buffers because the base voltage (output) "follows" the emitter voltage (input), hence the name "emitter follower". CC amplifiers provide high input impedance and low output impedance. This feature of impedance transformation can be utilized to implement impedance matching networks that contain active devices. Also, an emitter follower exhibits considerable current gain, therefore it is expected that the Cascode–CC topology will produce an amplifier power gain that is even greater than the Cascode.

Table 3.2 presents the DC operating points for the Cascode transistors of this architecture. These collector currents are slightly lower than their counterparts in Table 3.1 because of the lower collector-emitter voltage. Moreover, the CC stage transistor draws 552 $\mu$A of current, so the power consumption of the whole circuit increases only imperceptibly.

The schematic of the Cascode–CC topology is presented in Figure 3.14.
Table 3.2: Three bias points for the Cascode–CC topology for $V_{CE} = 1.2$ V

<table>
<thead>
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<th>$V_{BE}$ values</th>
<th>$I_C$ values</th>
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<td>2.52 mA</td>
</tr>
</tbody>
</table>

Figure 3.14: Unmatched Cascode–CC schematic ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)

On the other hand, Figure 3.15 shows the stability factors and the output impedances of the three different architectures side by side, in order to be compared to each other.

The value of the output shunt resistor and the value of the base-emitter voltage of the CC stage, in each topology, was tuned in order that an optimal trade-off between stability and output return loss could be achieved. In the first case, unconditional stability is not guaranteed for frequencies greater than 8.5 GHz, despite $\text{Re}\{Z_{out}\}$ being nearly $50\Omega$. In the second case, the
Figure 3.15: Stability performance and output impedance for three narrow-band Cascode topologies ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)
stability factor is above 1, whereas Re\{Z_{out}\} is positive.

So, although the extra transistor of the latter topology increases the DC power consumption, it was deemed necessary that unconditional stability for a frequency range larger than the operating bandwidth must be assured. Therefore, we shall proceed with the Cascode–CC architecture. The schematic of the amplifier along with the lumped-element matching networks is depicted in Figure 3.16.

![Figure 3.16: Cascode–CC schematic with matching networks (V_{BE} = 0.82 V, V_{CE} = 1.2 V)](image)

The simulation results of Figure 3.17 reveal that reverse isolation remains adequately high and the two-port network is unconditionally stable for frequencies lower than 10 GHz. In addition, the amplifier gain, |S_{21}|, has improved remarkably, having risen by almost 10 dB in comparison with the Cascode topology for the same DC bias point. As expected, gain and noise figure performance degrades within limits as \(I_C\) falls, too.
Hence, it was determined that the optimal Q-point for the transistors of the Cascode with which the design should be continued and that conforms with every design constraint is:

\[ V_{BE} = 0.82 \, \text{V}, \quad V_{CE} = 1.2 \, \text{V} \Rightarrow I_C = 3.61 \, \text{mA} \]
(a) $V_{BE} = 0.8425\, \text{V}, \; V_{CE} = 1.2\, \text{V}$

(b) $V_{BE} = 0.82\, \text{V}, \; V_{CE} = 1.2\, \text{V}$

(c) $V_{BE} = 0.81\, \text{V}, \; V_{CE} = 1.2\, \text{V}$

Figure 3.17: Matched narrowband Cascode–CC simulation results
Chapter 4

Broadband Low Noise Amplifier Design

Having discussed the narrowband design of the LNA in detail, this chapter will address techniques and methods for a broadband LNA design. In order for the RF front end to be able to handle a wide band of frequencies, several improvements must be made. For example, the matching networks must be able to accommodate the frequency-varying input and output impedances, in order to transform them to 50Ω. Also, another parameter that must be taken into account is gain flatness versus frequency. If there is substantial variation of the amplifier gain, then the various frequency components of the signal will be amplified unequally and its data might be corrupted.
4.1 Chebyshev Filters

In the following section, the basics of Chebyshev filters will be outlined. This type of filters is described by the transfer function $H_n(s)$ in equation (4.1):

$$G_n(\omega) = |H_n(j\omega)| = \frac{1}{\sqrt{1 + \varepsilon^2 T_n^2 \left( \frac{\omega}{\omega_0} \right)}}$$

(4.1)

where $T_n(\omega)$ is a $n$-th order Chebyshev polynomial. They are defined by the recurring relation (4.2).

$$T_0(x) = 1$$
$$T_1(x) = x$$
$$T_{n+1}(x) = 2xT_n(x) - T_{n-1}(x)$$

(4.2)

![Figure 4.1: Lumped-element Chebyshev Filter](image)

If lumped elements are utilized to realize a Chebyshev filter, then the component values for a low-pass prototype filter, such as the one shown in Figure 4.1, are equal to the $G_k$ ones. The latter are calculated by means of substi-
tution in equation (4.3).

\[ G_0 = 1 \]
\[ G_1 = \frac{2A_1}{\gamma} \]
\[ G_k = \frac{4A_{k-1}A_k}{B_{k-1}G_{k-1}}, \quad k = 2, 3, \ldots, n \]  \hspace{1cm} (4.3)
\[ G_{n+1} = \begin{cases} 1 & \text{if } n \text{ odd} \\ \coth^2 \left( \frac{\beta}{4} \right) & \text{if } n \text{ even} \end{cases} \]

where

\[ \gamma = \sinh \left( \frac{\beta}{2n} \right) \]
\[ \beta = \ln \left[ \coth \left( \frac{\delta \ln 10}{40} \right) \right] \]
\[ A_k = \sin \left( \frac{(2k - 1) \pi}{2n} \right), \quad k = 1, 2, \ldots, n \]
\[ B_k = \gamma^2 + \sin^2 \left( \frac{k \pi}{n} \right), \quad k = 1, 2, \ldots, n \]  \hspace{1cm} (4.4)

and \( \delta \) is the passband ripple in dB. The input and output impedances of the filter are assumed to be 50\( \Omega \). The low-pass prototype filter can be then transformed to a bandpass filter through two methods called "impedance scaling" and "frequency transformation". They are described in detail in [6].

![Figure 4.2: Lumped-element bandpass Chebyshev filter (4.5-7.5 GHz)](image-url)
The L-C components for any filter type and response can be handily computed via online calculators, e.g. RF Tools | LC Filters Design Tool. For example, if we are to design a bandpass Chebyshev filter with its bandwidth being 4.5-7.5 GHz and its passband ripple, $\delta$, being 0.1 dB, the online calculator above yields the circuit of Figure 4.2.

### 4.2 Broadband Matching Network

The proposed method for realizing broadband matching networks will be discussed below. The input and output impedances of active devices, such as the RF transistors used in this Cascode–CC topology, are often frequency-varying. However, the source and load of a Chebyshev filter may be approximated by an R-L-C resonant circuit. Then, the reactive part of the circuit can be assumed to be a section of a typical Chebyshev filter with resistive terminations, so the L-C component values can be calculated from equations (4.2) and (4.3).

![Diagram of input and output matching networks](image)

(a) Input matching network  (b) Output matching network

Figure 4.3: Lumped-element bandpass (4.5-7.5 GHz) Chebyshev matching networks

Subsequently, the input and output filters, that were designed to achieve
broadband matching for the Cascode–CC schematic in Figure 3.14, are depicted in Figure 4.3. Also, the schematic of the whole circuit and the corresponding simulation results are shown in Figure 4.4.

It is observed that the input and output return loss remain lower than -10 dB inside the frequency band of interest (4.5-7.5 GHz) as well as that the noise figure does not exceed 2.1 dB. However, gain variation is considerable, being approximately 2.7 dB, and unconditional stability is not guaranteed around 10 GHz. For the time being, the latter issue is not an insurmountable problem, because it is anticipated that microstrip conductor losses will raise the stability factor, $K$, and stability measure, $B_1$. Regarding gain flatness, a relevant broadband technique will be discussed in the next section.
Figure 4.4: Cascode–CC configuration with broadband lumped-element matching networks ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)
4.3 Interstage Matching Network

In order to counter the frequency roll-off of the LNA, without violating the DC power consumption constraint, a form of passive gain compensation is required. In [8], the technique of interstage compensated matching networks is introduced. A typical example of amplifiers that employ this technique is presented in Figure 4.5. Interstage matching networks mismatch the impedance at their input and output, thus producing a frequency response of $|S_{21}|$ with positive slope. As a result, the amplifier frequency response becomes flat and gain variation is reduced. To demonstrate this effect, a two-port network with a series and a shunt inductor and its S-parameter frequency response is shown in Figure 4.6. It should be pointed out that, while the impedances looking into the collector of transistor $Q_1$ and the emitter of $Q_2$ are not equal to 50 $\Omega$, the topology of Figure 4.6a operates in a likewise manner and yields the intended results. Figure 4.7 depicts the enhanced Cascode–CC configuration and its respective results.

The final simulation results are summarized below. The total DC power consumption of the LNA is equal to the sum of the power supplied by each
Figure 4.6: Interstage matching network with a series and a shunt inductor individual voltage source in the circuit. So, it holds that $P_{\text{DC}} = 9.597$ mW. Also, the amplifier gain is equal to $15.3 \pm 0.5$ dB, whereas the noise figure is equal to $1.85 \pm 0.15$ dB. Stability is ensured throughout the bandwidth of interest, that is, 4.5–7.5 GHz, but potential oscillations might arise at frequencies around 10 GHz. Lastly, input and output matching are up to mark; they are much lower than -10 dB.
Figure 4.7: Cascode–CC configuration with broadband lumped-element matching networks and interstage matching network ($V_{BE} = 0.82$ V, $V_{CE} = 1.2$ V)
Chapter 5

Phase Shifter Design

5.1 Phase Shifter Type

Due to the Printed Circuit Board being fabricated using microstrip, it was assessed that the best course of action is to realize a Reflection-Type Phase Shifter, instead of the alternative types of Phase Shifters summarized in section 2.3.1. Its passivity and layout simplicity attest its superior status for the present low-power application.

In the sections below, two possible architectures for the variable loads of the RTPS shall be proposed: a pi-network load and an LC resonant load. With regards to the 3-dB quadrature hybrid coupler, since various types of couplers have been addressed in section 2.3.1, its implementation will be considered on Chapter 6.
5.2 Variable Load Topology

5.2.1 Pi-Network Load

The first proposal for the variable load is based on the RTPS architecture developed in [7] and it is shown in Figure 5.1. It is indicated in [14] that controlling the phase shift through only one varactor diode leads to a strong dependency of insertion loss on phase shift. Thus, the pi-network load can help reduce it without compromising the goal of a full 360° phase control range. It consists of two varactor diodes, whose capacitances vary independently of each other as well as an intermediate inductor whose value is constant. To accommodate the needs of this application for an optimal trade-off between low $IL$ and high phase shift range, the capacitances span from 0.2 to 2.5 pF and the value of the inductor is 1.937 nH. A quality factor of $Q = 15$ is presupposed for both capacitors and inductors.

Since there are two independent variables which affect insertion loss and
phase shift behavior, it is convenient to plot contour lines for each quantity. They are plotted in Figure 5.2.

Figure 5.2: RTPS with pi-network load simulation results at 6 GHz

In lieu of a plot legend for Figure 5.2, a short description for the line colors will be given below:

Red and yellow lines indicate lower values:
\[
\begin{align*}
IL_{\text{dB}} &= 0.5, 1, \ldots \\
PS &= -180^\circ, -168.75^\circ, \ldots
\end{align*}
\]

Blue and cyan lines indicate higher values:
\[
\begin{align*}
IL_{\text{dB}} &= 6, 5.5, \ldots \\
PS &= 180^\circ, 168.75^\circ, \ldots
\end{align*}
\]

Table 5.1: Plot legend for Figure 5.2

Full phase control range of 360° is achieved, because there exist valid $S_{21}$ points for every angle in the Smith chart ($\Gamma$ plane). Also, due to the wraparound of the two capacitance values, phase shift cannot be continuously controlled by the control voltages of varactor diodes. Thus, phase shift
is shown in $11.25^\circ$ increments in Figure 5.2, i.e. the phase resolution of this phase shifter is $11.25^\circ$. A potential method of finding the voltage pairs that correspond to each phase-shift step is to choose a suitable constant-$IL$ contour line and intersect it with the phase-shift ones. The leftmost contour plot presents the intersections of both types of $IL$ and phase-shift contour lines that yield the aggregate of the pairs of the control voltages which in turn produce the $11.25^\circ$ intervals of the full-360$^\circ$ phase control range.

Although the above method is concise in identifying voltage values for a desired insertion loss level and phase shift, its main disadvantage is that a varactor with a $C_{\text{max}}/C_{\text{min}}$ of at least 15 is required. Such values are virtually unfeasible to realize in fabrication processes of varactor diodes, therefore a phase control range of 360$^\circ$ cannot be achieved in practice. Moreover, the insertion loss specifications that were set in the beginning of the Thesis cannot be realized for a wide bandwidth, e.g. for 4.5 GHz through 7.5 GHz. This is a consequence of the lumped nature of the inductors and capacitors involved. Finally, the control voltage pairs that would be selected to produce the desired phase shifts with acceptably low insertion loss for a single frequency point cannot be reused to reproduce the same phase shifts in different frequencies of the operating bandwidth.
5.2.2 LC Resonant Load

The second load topology, which is based on [4], is presented in Figure 5.3. Per [5], the leftmost inductors, that are resonating with the varactor diodes, are responsible for an increased phase range. Combining two such LC loads so that they are in parallel yields an additional phase range increase. Lastly, insertion loss fluctuations relative to frequency are reduced by attaching a
low-pass matching LC network, as evidenced by the motion of the center of the $\Gamma_L$ circle towards the origin of the Smith chart. The successive effects of each component on the reflection coefficient of the variable load are shown in Figure 5.4. For the purposes of the S-parameter simulation, a quality factor of 15 and 30 was assumed for each inductor and capacitor, respectively.

The results of a 6 GHz simulation for the ideal RTPS topology, presented in Figure 5.5, show that the phase control range exceeds 360° and the maximum value of insertion loss is lower than 4 dB. Simultaneously, the $C_{\text{max}}/C_{\text{min}}$ ratio equals to 5, since the varactor capacitance ranges from 0.3 pF to 1.5 pF. Additionally, a single voltage source is implemented in this topology to vary the diode capacitance. As such, the complexity of the computer and DAC that will handle the appropriate control signals is lower than the one involved in the case of the RTPS with pi-network loads.

Figure 5.5: RTPS with LC-resonant loads simulation results at 6 GHz
5.3 Varactor Diode Model Selection

In this stage of the Thesis, an appropriate model for a varactor diode must be chosen, so that to incorporate any parasitic elements of the component package or the diode process into the S-parameter simulations. After an extensive search for a varactor diode that satisfies the need for a capacitance range of 0.1 pF through 1 pF, we arrived at the MACOM’s MA46H120 series. It is a GaAs flip chip hyperabrupt varactor diode with a zero-bias junction capacitance, $C_{j0}$, equal to 1.09 pF and capacitance range approximately equal to 0.9 pF. Its quality factor, $Q$, equals to 3000 at 50 MHz.

![Schematic and S-parameter simulation results](image)

(a) Schematic

(b) S-parameter simulation results

Figure 5.6: MACOM MA46H120 equivalent circuit

The manufacturer of this varactor provides an equivalent circuit that may be used for the necessary S-parameter simulations in ADS. It includes both the parasitic capacitance of the package and the parasitic inductance due to the bond wire connecting the anode of the package with the varactor die. The corresponding schematic is presented in Figure 5.6a. The diode capacitance exhibited in Figure 5.6b varies between 0.2 pF and 1.2 pF versus the level of the DC control voltage. As a result, this varactor diode series is fit for use
in the present phase shifter topology.

The phase shifter configuration presented in section 5.2.2 shall be modified accordingly to factor in the parasitics of the varactor diode model as represented by the schematic of Figure 5.6a. In Figure 5.7, the various component specifications were fine-tuned in order to achieve low insertion loss and full phase range anew. The results of the S-parameter simulation in this occasion are outlined in Figure 5.8. Similarly to Figure 5.5, insertion loss remains lower than 4 dB and the available phase control range surpasses 360°. Also, the group delay of the system is less than 1 ns, meaning that the amplitude envelope of the input signal does not suffer from noteworthy time delay.

![Figure 5.7: Schematic of the modified RTPS with LC-resonant loads](image-url)
5.4 RTPS Topology with LC Loads and Two Couplers

Although the RTPS topology with a single quadrature 3-dB hybrid coupler of Figure 5.7 yields adequate phase range and insertion loss results, it is expected that the narrowband nature of the LC components will worsen its performance during the PCB design stage. A possible solution to this issue would be to independently tweak the load impedances of the through and coupled ports of the coupler in order to obtain a satisfactory system response. However, this process requires explicit formulae for the phase control range and insertion loss as functions of the load components, which are strenuous.
Figure 5.9: Schematic of a RTPS with two quadrature 3-dB hybrid couplers [10]

to extract and might not model the RTPS behavior precisely. Also, the time complexity of an optimization routine to provide the optimal LC values would be great, due to the number of independent variables, thus this method was abandoned.

As a result, a new RTPS topology is presented in Figure 5.9, which is originally found in [10]. This configuration relaxes the constraints for a full 360° phase range by utilizing two hybrid couplers. Each phase shifter stage, then, is responsible for producing 180° of maximum phase shift with low insertion loss and low insertion-loss variation. The two cascaded stages are symmetrical so that the design flow is identical to the one outlined in this Chapter.

Since the design flow on a schematic level has essentially finished, it would be redundant to simulate the double-coupler RTPS with ideal lumped components at this point. As it will be shown below, it is convenient to simplify the load by removing one of the two parallel LC resonant branches in series with the "matching" network. Consequently, the new modifications will be
presented in Chapter 6 along with the transformation of the lumped elements to transmission lines.
Chapter 6

Printed Circuit Board Design

In this Chapter, the procedures with which the RF front end’s lumped and ideal components will be transformed to transmission lines shall be presented. Afterwards, the layout of the final circuit will be constructed and altered accordingly so that it includes:

- the substrate and conductor connections materializing the transmission lines in the form of microstrip,
- footprints for the discrete inductors, capacitors and varactor diodes, i.e. conductive points upon which they will be soldered and interfaced with the microstrip,
- bias networks that will be connected to DC voltage sources and decouple them from the rest of the circuit, and
- vias that will realize grounding and facilitate robust RF current return paths.
The necessary simulations are provided by Keysight’s Momentum. It is a 3D planar EM simulator which discretizes arbitrary geometrical shapes into cells before it calculates the electric and magnetic surface currents for each one of them. The technique is called Method of Moments (MoM) and is based on [9].

6.1 PCB Substrate

Figure 6.1: Substrate layer stackup for this design

It is expedient to start this stage of the design process by selecting a PCB substrate with specifications that meet the goals of the Thesis. For this reason, it was concluded that PCB laminates from Rogers Corporation are the most reliable due to the company’s renown in the market. Finally, the winning candidate was the Rogers RT/duroid 5880 laminate series because of its low dielectric constant of 2.2, minuscule loss tangent of 0.0009 at 10 GHz and uniform broadband performance.

The thickness of the substrate was selected to be 20 mil, in order for the transmission lines length not to be too high. Also, the first conductor layer, denoted by ”cond” in Figure 6.1, was chosen to be 1.3 mil thick. On the other hand, ”cond2” refers to a second conductor layer that will only be utilized
for the purpose of constructing the air bridges of Lange couplers.

6.2 Modifications to the Low Noise Amplifier

Before the matching-network components are transformed into distributed elements, it is fitting to select a suitable discrete DC-block capacitor model to replace its ideal counterpart in the schematic diagram. Discrete capacitors have frequency-dependent behavior due to parasitic inductances and capacitances caused by their package. As a result, there is a certain frequency value, called the Series Resonant Frequency (SRF), above which the capacitor will act as an inductor. This alternating capacitive-inductive behavior is periodic and is repeated every PRF Hz. PRF stands for Parallel Resonant Frequency and above this frequency the capacitor’s transmission impedance becomes too high for proper usage. PRF is double the SRF, according to a common rule of thumb [22]. A insertion loss versus frequency plot for a typical capacitor is depicted in Figure 6.2. Each impedance trough occurs when the reactive elements of the capacitor cancel each other out and its reactance is zero. The first trough happens when $f = \text{SRF} \, \text{Hz}$.

6.2.1 Introduction of an SMD Capacitor

The capacitor that was chosen for the LNA stage is Murata’s GRM0225C1E9R5WA03 ceramic SMD capacitor with a capacitance of 9.5 pF and an SRF of approximately 4 GHz. Due to the introduction of the capacitor in the circuit, it is anticipated that the input and output impedances of the amplifier stage, excluding the matching networks, will change slightly.
Thus, the input and output matching networks were appropriately tweaked, so that the desired specifications are attained. The schematic diagram of the updated circuit and its S-parameter simulation results can be seen in Figures 6.3 and 6.4. These results are comparable to the ones in Figure 4.7.
This subsection relies heavily on the broadband matching technique described in subsection 2.2.3. The lumped matching networks that were designed above shall be transformed according to the formulae in Figure 2.13. The width and length of the microstrip transmission lines are calculated by the $Z_o$ and $\theta$ values, where $\theta$ is the electrical length of the transmission line measured in rads or degrees through Keysight’s LineCalc program, which is included in Keysight’s Advanced Design System. It is of particular interest to note that the aforementioned equations hold true only in a narrow frequency band. Therefore, the distributed elements are synthesized at 6 GHz and will subsequently be fine-tuned in order to achieve matching in the 4.5–7.5 GHz region. In order not to have extremely large microstrip dimensions, the widths and lengths of the lines were kept between 10 mil and 400 mil.

After multiple iterations of the above method, that is to say, after continuously fine-tuning the dimensions of the transmission lines after their syn-
thesis, the synthesized matching networks are shown in Figures 6.5 and 6.6. Attention was given to the fact that the widths of the emitter inductance as well as the interstage matching network transmission lines should be equal to the width of the transistor footprint, in order not to aggravate the am-

Figure 6.5: Schematic diagram of the LNA stage with distributed matching networks

Figure 6.6: Simulation results for the LNA stage with distributed matching networks
plifier’s response through mismatched line impedances. Also, the DC-block SMD capacitor was placed to the right side of the output matching network, since the emitter of the CC transistor is always a DC ground. Furthermore, a DC path between a varactor control voltage and another grounding point may be created by the topology of the quadrature hybrid coupler, hence the need for decoupling.

Input and output return loss as well as noise figure has moderately deteriorated, because of the narrowband behavior of microstrip transmission lines. On the other hand, the stability factor is now above unity, ensuring unconditional stability. This can be attributed to ohmic losses of the microstrip, which attenuate unwanted oscillations in the two-port network.

6.3 Modifications to the Phase Shifter and RF Front End Results

Turning to the Phase Shifter, a few modifications will be made to the LC loads in order that the layout design be foolproof at its later stage. Firstly, the lumped “matching” network components will be transformed to distributed accordingly. Their width has been chosen to be 62 mil, which results in 50Ω lines, in order to match the width and characteristic impedance of the lines of the quadrature hybrid coupler. Secondly, the inductance resonating with the varactor has been moved to the right of the diode, so that the through-hole via does not overlap with the varactor diode and its footprint. Lastly, another DC-block capacitor is needed at the network output, because large currents were detected at that point due to an unwanted DC path. The
exact capacitor model will be chosen after the coupler topology has been determined, so an ideal DC-block capacitor will be used for the S-parameter simulation in this section.

Figure 6.7 shows the full RF front end with both the modified LNA stage of section 6.2 and the above-mentioned PS, whereas Figure 6.8 outlines the S-parameter simulation results for this configuration. The phase range is higher than 360°, gain variation is equal to almost 2 dB and the two-port network remains unconditionally stable. Additionally, marker "m2" indicates that amplitude distortion is low at 1.1 dB, while marker "m1" shows that for a given phase shift value, or equivalently, for a given control voltage, the maximum deviation of the power gain is ±1 dB.

Figure 6.7: Schematic diagram of the modified LNA–PS with distributed matching networks
6.4 Design Using Keysight’s Momentum

In this section, we shall proceed with the construction of the PCB layout and the EM simulations of the LNA–PS with Keysight’s Momentum RF simulator.

Point pins were predominantly used for the network ports, since [17] shows that edge or area ports do not improve simulation results. Also, the port calibration mode is set to "TML" when a port is connected to a transmission line, so that the open ended line discontinuity effects are removed and mutual coupling between parallel lines is not taken into account. Otherwise, the calibration mode is set to "Direct", when, for example, the port is connected to a two-terminal device or a transistor.
6.4.1 Component Footprints

First of all, footprints must be affixed to the terminal points of each discrete component that is utilized in the circuit. Their dimensions were extracted from their respective datasheets and their layout view is depicted in Figures 6.9 and 6.10. In the case of the RF transistor, although its two emitters are wire-bonded, it would be preferable not to have one of them as a floating node in the circuit. Thus, a small microstrip section was added to the transistor footprint in order to short-circuit the two emitters. The conductor thickness is much smaller than the transistor’s package height, so that is a realizable solution. The inclusion of footprints resulted in very subtle changes to the performance of the LNA.

![Figure 6.9: Footprints for the discrete components](image)

- (a) Capacitor
- (b) Inductor
- (c) Varactor diode

![Figure 6.10: Footprints for the RF transistor](image)

- (a) Datasheet footprint
- (b) With short-circuited emitters
6.4.2 Matching networks

The matching networks of Figure 6.7 were enhanced by the addition of a T-Junction so that discontinuities between the line widths are accounted for. As a result, several optimizations by hand were made in order to take the T-Junction into account and achieve satisfactory input and output matching. The layout of the input and output matching networks is seen in Figure 6.11. This Figure also shows the layout mesh whose density was set to 20 cells/wavelength so that the simulation time did not become unreasonably high.

![Input matching network](image1) ![Output matching network](image2)

Figure 6.11: Layouts of the matching networks of the LNA

This process is repeated throughout the following subsections, because the introduction of parasitics by the microstrip lines, e.g. the bias feed lines and vias, alters the response of the filters, thus Momentum RF EM simulation results for the LNA will be presented at the end of this section.

Similarly, the layout of the interstage matching network and the degeneration inductance were designed accordingly and were incorporated in the final layout design.
6.4.3 Bias Networks

The bias feed networks, such as the one in Figure x are essentially $\lambda/4$ high-impedance transmission lines. The property of the quarter-wave impedance transformer prevents the bias line from loading the RF circuit, since the square pad, where 2.54mm pin headers will be placed to facilitate the connection of the DC voltage sources, acts as a low-impedance line. Hence, the small width of the bias lines and the larger width of the square pads. Concerning the RF path between the cascode and the CC stages, a simple $\lambda/4$ transmission line was unable to behave as an RF choke inductor, due to the adjacent placement of the two DC feed inductors and the intermediate DC block capacitor. Therefore, two SMD inductors—Murata’s LQP03HQ18NH02—precede each bias transmission line and are placed between Murata’s GRM0225C1E9R5WA03 decoupling capacitor.

Figure 6.12: Bias network
6.4.4 Vias and Low Noise Amplifier Results

The through-hole vias used in this PCB are identical to the one pictured in Figure 6.13. Before the hole is drilled through the board, a sufficiently large annular pad must enclose the designated area for said hole. Afterwards, the outer part of the via is usually plated with conductive material, whereas the inner part is filled with a non-conductive material, which is often air. In this application, the side of the annular pad is equal to 25 mil and the hole diameter is equal to 15 mil. The metal thickness is the same with the microstrip conductor; 1.3 mil.

The combined simulation results of the Momentum RF simulator for the LNA stage are shown in Figures 6.14 and 6.15. An SMA connector was added to the input of the LNA stage so that to interface the circuit with coaxial cables. In order not to alter the response of the input matching network with the addition of the SMA connector, a \( \lambda/2 \) transmission line was included, too. The input return loss is slightly below 10 dB and output matching is satisfactory. The stability concerns over the frequency band of interest are allayed due to the introduction of a 10 \( \Omega \) resistor between the emitter of the Common Collector transistor and the output matching network, apart from
1.5 GHz where the stability factor is 0.18. Also, the gain variation versus frequency and the noise figure have marginally increased, especially around 7 GHz but are within acceptable limits.

6.4.5 Quadrature 3-dB Hybrid Coupler Realization

Turning to the layout of the Phase Shifter, the topology of the quadrature coupler that will replace the ideal model of the schematic must be determined beforehand. Following the conclusions of subsection 2.4, it was decided that a Lange coupler was the most appropriate type of 3-dB coupler for the present application. The number of fingers was chosen to be the lowest possible, \( N = 4 \), because the coupling factor becomes more sensitive to the width and

Figure 6.14: LNA stage layout schematic diagram

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gaps of the fingers, as $N$ increases. The length of each finger ought to be $\lambda/4$ at the center frequency, which is 6 GHz in this case. In order to achieve the 3-dB coupling, the finger width and gaps were adjusted in such manner as to keep the finger spacings above 1 mil. So, we arrived at the coupler of Figure 6.16a, with a finger width of $W = 10.996$ mil, finger gap of $S = 1.17$ mil and finger length of $L = 377.677$ mil. Instead of bond wires, air bridges were placed in the appropriate spots to actualize the connections between the Lange coupler’s fingers. The structure of the air bridges used in this coupler is shown in Figure 6.17. It consists of a conductor layer that is on the top of the first one as well as a perpendicular conductor that acts as a transition between the two layers. While this is not the case in this coupler implementation, air bridges are usually supported by polyimide which keeps
the bridge height constant throughout fabrication and averts potential short circuits. Overall, the phase difference between the through and coupled ports is approximately equal to 91° and the coupling factor in the frequency band of interest ranges from 2.5 dB to 4.6 dB.

Figure 6.16: Lange quadrature 3-dB hybrid coupler

Figure 6.17: Air bridge detail for the present Lange coupler
6.4.6 Phase Shifter Layout

Having resolved the topology of the hybrid coupler, we shall merge it with the variable loads that were designed in section 6.3 and vias in order to simulate the Phase Shifter in its entirety.

![Phase Shifter schematic diagram](image)

Figure 6.18: Phase Shifter schematic diagram

The results of Figure 6.19, which correspond to the Phase Shifter depicted in Figure 6.18, demonstrate that, whereas the phase range surpasses 349°, the minimum input and output return loss deteriorates at certain control voltage values for frequencies above 5 GHz. This effect is attributed to the large voltage swing of the voltage sources of the varactor diodes which cause large mismatching on the through and coupled ports. As a result of this, the impedance presented to the input and isolated ports of the coupler deviates...
largely, hence the low input and output return loss.

6.4.7 Final LNA–PS PCB Layout

The final printed circuit board for the RF front end is presented in Figure 6.20 whilst its respective simulation results are shown in Figure 6.21.

First of all, the 10 Ω resistor proved to be redundant since unconditional stability is ensured without its inclusion. Also, the variable loads of the Phase Shifter and its vias were realized and added to the PCB. Another SMA connector and half-wave transmission line was added to the output of the system as well as a decoupling capacitor to tackle an undesirable DC
Figure 6.20: LNA–PS layout view
Figure 6.21: LNA–PS simulation results
path facilitated by the Lange couplers. The capacitor model is Murata’s GRM1555C1H101JA01. Moreover, the Lange couplers were rotated appropriately so that their placement minimizes the PCB area as much as possible.

Noise Figure remains low with a maximum of 1.787 dB at 7.5 GHz and the circuit is stable even after the removal of the series 10 Ω resistor. Despite the fact that input return loss is lower than 10 dB at frequencies higher than 7.3 GHz, the maximum reflected power at 7.5 GHz is less than 15.85% of the total input power. On the other hand, output matching is out of bounds as explained in subsection 6.4.6. However, it is deemed that this compromise was required to achieve a phase control range of more than 354° at the frequency band of 4.5–7.5 GHz. Although, gain variation is considerable, the minimum gain attained by this RF front end exceeds 13 dB. Lastly, the PCB area is 9.42 cm × 2.31 cm.

In order for the PCB design to be complete, a ground plane with vias placed periodically must be fitted on the first layer. Per [12], the gap between each microstrip trace and the top ground plane is given by

\[ G = 1.5H + \frac{H}{W} + \frac{20}{\varepsilon_r} \]  

(6.1)

The gap value was thus determined to be at least 45 mil. The resulting layout of the LNA–PS with the top ground plane is shown in Figure 6.22. It is expected that the S-parameter simulation results will not differ from the ones presented in Figure 6.21.
Figure 6.22: LNA–PS layout view with a top ground plane
Chapter 7

Conclusion

In conclusion, a low-power 4.5–7.5 GHz RF receiver front end encompassing a Low Noise Amplifier and a Phase Shifter was designed for the purposes of this Thesis. After a thorough description of basic notions of RF/Microwave Design in Chapter 2, a suitable transistor was chosen to realize the LNA according to the design goals. Rudimentary topologies such as the Common Emitter and Cascode were formed and simulated, and as a result, the most qualified topology that balances low power with robust amplifier specifications was determined to be the Cascode–CC configuration. The next order of business was to appropriately modify the matching networks of the LNA as well as introduce an interstage network so as to achieve a broadband amplifier response along the 4.5–7.5 GHz band. Thereafter, the PS topology was considered, where a reflective-type PS with variable LC loads was found to produce the optimal trade-off between its insertion loss and phase control range. Subsequently, the layout for the LNA–PS was constructed and augmented with bias networks and vias as well as SMA connectors that interface
it with the outside world. As a result, the LNA–PS yields the results outlined in Table 7.1.

<table>
<thead>
<tr>
<th>Measures</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure</td>
<td>1.2-1.8 dB</td>
</tr>
<tr>
<td>LNA-PS Gain</td>
<td>12.5-20 dB</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>8.6-17 dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>2.1-34 dB</td>
</tr>
<tr>
<td>Stability Factor</td>
<td>&gt; 1.4</td>
</tr>
<tr>
<td>LNA DC power consumption</td>
<td>9.6 mW</td>
</tr>
<tr>
<td>Phase Control Range</td>
<td>354.3°-420.6°</td>
</tr>
<tr>
<td>Phase Shift slope vs. freq. @ 6 GHz</td>
<td>-194.4°</td>
</tr>
<tr>
<td>PCB Area</td>
<td>9.42 cm × 2.31 cm</td>
</tr>
</tbody>
</table>

Table 7.1: Results of the final LNA–PS

Certain improvements to the present circuit can be made. For example, variable-gain amplifiers should be added in order to tackle the issue of amplitude distortion due to the considerable gain variation. Moreover, dedicated biasing circuits, e.g. current mirrors or bandgap reference circuits, can potentially be added to provide temperature-independent DC voltages. Lastly, a metal case must be fitted around the PCB that will provide ESD protection to the sensitive RF components and will act as a Faraday cage which will protect the circuit from unacceptable interference.
Bibliography


